Listing of claims:

1. (Currently Amended) A random access memory device ~~in an integrated circuit chip~~, comprising:

a memory array of memory cells organized into rows and columns, including a plurality of word lines and bit lines, each row of memory cells being coupled to a word line and each column of memory cells being coupled to a bit line;

sense amplifier circuitry coupled to the bit lines and being selectively disabled;

address decode circuitry for receiving an address value and asserting a row line associated therewith; and

test circuitry, coupled to at least one bit line, for placing on an external pad of the integrated circuit chip a current level corresponding to a voltage level appearing on the at least one bit line, ~~while concurrently disabling the sense amplifier circuitry~~ the test circuitry comprising:

a plurality of pairs of series-connected transistors coupled between the external pad and a reference voltage level, each pair of series-connected transistors including a first transistor having a control terminal coupled to a distinct one of the plurality of bit lines.

2. (Original) The random access memory device of claim 1, wherein the random access memory device comprises a ferroelectric memory device.

3. (Original) The random access memory device of claim 1, wherein the random access memory device comprises a nonvolatile memory device.

4. (Original) The random access memory device of claim 1, wherein the sense amplifier selectively drives the bit lines towards high and low reference voltage levels during normal memory access operations, the random access memory device is selectively configured in a test mode of operation by the test circuitry, and the sense amplifier circuitry is disabled from driving the bit lines by the test circuitry when the random access memory device is in the test mode of operation.

5. (Original) The random access memory device of claim 4, wherein the random access memory device includes a test input signal and is selectively configured in the test mode of operation based upon a value of the test input signal.

6. (Canceled).

7. (Canceled).

8. (Currently Amended) The random access memory device of claim 1, wherein the external pad is sized for external test connection ~~to contact and electrically connect to a tester probe, and the test circuitry comprises a plurality of pairs of series connected transistors coupled between the pad and a reference voltage level, each pair of series connected transistors including a first transistor having a control terminal coupled to distinct bit line~~.

9. (Currently Amended) The random access memory device of claim 1 ~~8~~, wherein each pair of series-connected transistors comprises a second transistor having a control terminal connected to a control signal that selectively activates the second transistor.

10. (Original) The random access memory device of claim 9, further comprising a selection circuit that selectively activates the second transistors of the plurality of pairs of series-connected transistors in a sequential manner.

11. (Currently Amended) The random access memory device of claim 10, wherein the selection circuit comprises counter circuitry and decode circuitry having a plurality of output signals such that each output signal is connected to the control terminal of a distinct one of the second transistors in each of the plurality of pairs of series connected transistors ~~transistor~~.

12. (Currently Amended) A random access memory device, comprising:

a memory array of memory cells organized into rows and columns, including a plurality of word lines and bit lines, each row of memory cells being coupled to a word line and each column of memory cells being coupled to a bit line;

sense amplifier circuitry coupled to the bit lines and being selectively disabled;

address decode circuitry for receiving an address value and asserting a row line associated therewith; and

test circuitry, coupled to at least one bit line, for placing on an external pad of the integrated circuit chip a current level corresponding to a voltage level appearing on the at least one bit line ~~The random access memory device of claim 1~~, wherein the test circuitry comprises:

a first pair of series-connected transistors connected between the external pad of the integrated circuit chip and a reference voltage level, a first transistor of the first pair of series-connected transistors having a control terminal connected to the at least one bit line; and

a second pair of series-connected transistors connected between a test ~~second~~ pad of the integrated circuit chip and the reference voltage level, a first transistor of the second pair of series-connected transistors having a control terminal connected to a calibration ~~third~~ pad of the integrated circuit chip and a second transistor of the second pair of series-connected transistors being activated.

13. (Currently Amended) A random access memory device, comprising:

a memory array of memory cells organized into rows and columns, including a plurality of word lines and bit lines, each row of memory cells being coupled to a word line and each column of memory cells being coupled to a bit line;

sense amplifier circuitry coupled to the bit lines and being selectively disabled;

address decode circuitry for receiving an address value and asserting a row line associated therewith;

test circuitry, coupled to at least one bit line, for placing on an external pad of the integrated circuit chip a current level corresponding to a voltage level appearing on the at least one bit line; and ~~The random access memory device of claim 1, further comprising:~~

calibration test circuitry for providing a matching relationship between the current level placed on the external pad and the voltage level appearing at the at least one bit line.

14. (Currently Amended) The random access memory device of claim 13, wherein the test circuitry has a portion for placing having an electrical structure and the calibration test circuitry has substantially the same electrical structure as [~~a~~] the portion for placing of the test circuitry.

15. (Currently Amended) The random access memory device of claim 13, wherein the calibration test circuitry comprises:

an input connected to a ~~second~~ calibration external pad for externally controlling the operating characteristics of the calibration circuit; and

an output connected to a ~~third~~ test external pad for externally measuring a current flowing through the calibration test circuitry.

Claims 16-21. (Canceled)

22. (Currently Amended) An apparatus, comprising:

a random access memory device, comprising:

a memory array of memory cells organized into rows and columns, including a plurality of word lines and bit lines, each row of memory cells being coupled to a word line and each column of memory cells being coupled to a bit line;

sense amplifier circuitry coupled to the bit lines;

address decode circuitry for receiving an address value and asserting a row line associated therewith; and

test circuitry, coupled to at least one bit line for placing on an external pad during a test mode of operation a current level corresponding to a voltage level appearing on the at least one bit line, ~~the sense amplifier circuitry, including sense amplifier circuitry coupled to the at least one bit line, being disabled during the test mode of operation~~ the test circuitry comprising:

a pair of series-connected transistors coupled between the external pad and a reference voltage level, the pair of series-connected transistors including a first transistor having a control terminal coupled to the at least one bit line.

23. (Original) The apparatus of claim 22, wherein the random access memory device comprises a ferroelectric memory device.

24. (Original) The apparatus of claim 22, wherein the random access memory device comprises a nonvolatile memory device.

25. (Original) The apparatus of claim 22, wherein the random access memory device comprises sense amplifier circuitry that selectively drives the bit lines towards high and low reference voltage levels during normal memory access operations, the random access memory device is selectively configured in a test mode of operation by the test circuitry and the sense

amplifier circuitry is disabled from driving the bit lines by the test circuitry when the random access memory device is in the test mode of operation.

26. (Original) The apparatus of claim 22, wherein the apparatus further comprises:

a processing unit having an address port connected to an address input port of the random access memory device and a data port connected to a data port of the random access memory device.

27. (Currently Amended) The apparatus of claim 22, wherein the external pad is sized for external test connection ~~to receive a tester probe, and the test circuitry comprises a pair of series-connected transistors coupled between the external pad and a reference voltage level, the pair of series-connected transistors including a first transistor having a control terminal coupled to the at least one bit line~~.

28. (Currently Amended) The apparatus of claim 22 ~~27~~, wherein the pair of series-connected transistors further comprises a second transistor having a control terminal connected to a control signal that selectively activates the second transistor.

29. (Currently Amended) The apparatus of claim 22, wherein ~~the external pad is sized to receive a tester probe, and~~ the test circuitry comprises a plurality of pairs of series-connected transistors coupled between the external pad and a reference voltage level, each pair

of series-connected transistors including a first transistor having a control terminal coupled to a distinct one of the plurality of bit lines ~~line~~.

30. (Original) The apparatus of claim 29, wherein each pair of series-connected transistors comprises a second transistor having a control terminal connected to a control signal that selectively activates the second transistor.

31. (Original) The apparatus of claim 30, wherein the test circuitry comprises a selection circuit that selectively activates the second transistors of the plurality of pairs of series-connected transistors in a sequential manner.

32. (Original) The apparatus of claim 31, wherein the selection circuit comprises counter circuitry and decode circuitry having a distinct output signal connected to the control terminal of each of the second transistors.

33. (Currently Amended) The apparatus of claim 22, wherein the test circuitry further comprises:

~~a first pair of series-connected transistors connected between the external pad of the apparatus and a reference voltage level, a first transistor of the first pair of series-connected transistors having a control terminal connected to the at least one bit line; and~~

a second pair of series-connected transistors connected between a ~~second~~ test pad of the apparatus and the reference voltage level, a first transistor of the second pair of series-connected

transistors having a control terminal connected to a ~~third~~ calibration pad of the apparatus and a second transistor of the second pair of series-connected transistors being activated.

34. (Currently Amended) The apparatus of claim 22, wherein the random access memory device further comprises:

calibration test circuitry for providing a matching relationship between the current level and the voltage level appearing at the at least one bit line.

35. (Currently Amended) The apparatus of claim 34, wherein the test circuitry has a portion for placing having an electrical structure and the calibration test circuitry has substantially the same electrical structure as [~~a~~] the portion for placing of the test circuitry.

36. (Currently Amended) The apparatus of claim 34, wherein the calibration test circuitry comprises:

an input connected to a ~~second~~ calibration external pad for externally controlling the operating characteristics of the calibration circuit; and

an output connected to a ~~third~~ test external pad for externally measuring a current flowing through the calibration test circuitry.

37. (Currently Amended) An apparatus, comprising:

a ferroelectric capacitor; and

means for placing on an external pad of the apparatus during a test mode of operation a current level corresponding to a voltage level appearing across the ferroelectric capacitor, said means comprising a first transistor having a control terminal coupled to a plate of the ferroelectric capacitor, a first conduction terminal coupled to the external pad and a second conduction terminal ~~connected to a voltage reference~~, and a second transistor having a first conduction terminal connected to ~~the external pad~~ a voltage reference and a second conduction terminal connected to the ~~first~~ second conduction terminal of the first transistor, and a means for selectively activating the second transistor during the test mode of operation.

38. (Canceled).

39. (Canceled).

40. (Previously Added) The random access memory device of claim 1, wherein the current level placed on the external pad by the test circuitry is proportional to the voltage level appearing on the at least one bit line.

41. (Previously Added) The method of claim 16, wherein the current level provided to the pad is proportional to the voltage level appearing on the selected bit line.

42. (Previously Added) The apparatus of claim 22, wherein the current level placed on the external pad is proportional to the voltage level appearing on the at least one bit line.

43. (Previously Added) The apparatus of claim 37, wherein the current level placed on the external pad by the means for placing is proportional to the voltage level appearing across the ferroelectric capacitor.

44. (Previously Added) The apparatus of claim 37, wherein the plate of the ferroelectric capacitor is coupled to a column line, and the control terminal of the first transistor is connected to the column line.

45. (Currently Amended) The apparatus of claim 37, further comprising a ~~counter~~ control counting circuit having an output coupled to a control terminal of the second transistor.

46. (Previously Added) The apparatus of claim 37, further comprising a sense amplifier coupled to the plate of the ferroelectric capacitor, and wherein the means for placing further comprises a disable circuit for disabling the sense amplifier when the current level is placed on the external pad during the test mode of operation.

47. (Currently Amended) The apparatus of claim 37, further comprising calibration circuitry comprising a third transistor having a first conduction terminal coupled to a ~~second~~ test external pad, a second conduction terminal and a control terminal coupled to a ~~third~~ calibration external pad, and a fourth transistor having a first conduction terminal connected to the second conduction terminal of the third transistor, a second conduction terminal connected to the

voltage reference and a control terminal coupled to a voltage level to activate the fourth transistor.

48. (Previously Added) The apparatus of claim 47, wherein the third and fourth transistors substantially match the first and second transistors, respectively.

49. (Previously Added) The apparatus of claim 47, wherein the third and fourth transistors have substantially the same operating characteristics as the first and second transistors, respectively.